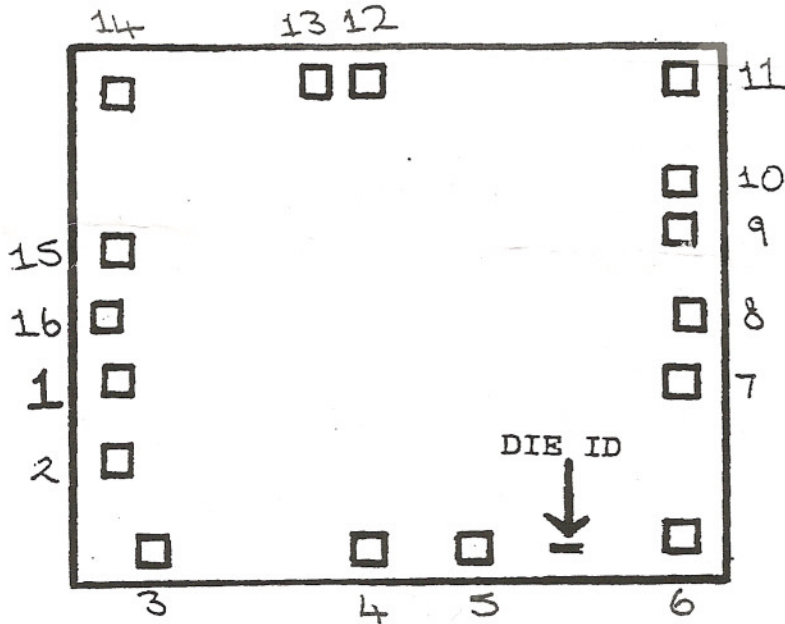




Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
 Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



| <u>Pad</u> | <u>Function</u> | <u>Pad</u> | <u>Function</u> |
|------------|----------------------|------------|----------------------|
| 1 | T _{1A} | 9 | Q _B OUT |
| 2 | T _{2A} | 10 | Q _B OUT |
| 3 | C _{DA} | 11 | B _B INPUT |
| 4 | A _A INPUT | 12 | A _B INPUT |
| 5 | B _A INPUT | 13 | C _{DB} |
| 6 | Q _A OUT | 14 | T _{2B} |
| 7 | Q _A OUT | 15 | T _{1B} |
| 8 | V _{SS} | 16 | V _{DD} |

Top Material:
Backside Material:
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY:MG

DIE SIZE :89 x 77

DATE: 10/28/08

MFG:NSC

THICKNESS:15

P/N:CD4538 BH